CLAIMS

What is claimed is:

1. A method of aligning a mask with a semiconductor wafer surface, comprising the steps of:

providing a semiconductor surface with one or more wafer alignment marks thereon;

providing a mask with one or more etchings effective in generating one or more 0-π-phase-conflict alignment marks under ambient lighting conditions of use;

wherein each said wafer alignment mark is of a geometry that is compatibly aligning with a corresponding 0-π-phase-conflict alignment mark; and

aligning said 0-π-phase-conflict alignment marks with their corresponding wafer alignment marks.

2. The method of claim 1 wherein said ambient lighting conditions comprise an illumination wavelength of from about 150 to about 450 nanometers.

3. The method of claim 2 wherein said wavelength is about 193 nanometers.

4. The method of claim 3 wherein said one or more etchings comprise a depression about 48 nanometers in depth.

5. A 0-π-phase conflict mask, comprising:

a mask comprising a transparent base material, having at least one depression etched thereon, said depression effective in generating a 0-π-phase-conflict mark under ambient lighting conditions of use.

6. The mask of claim 5 wherein said ambient lighting conditions comprise a wavelength of from about 150 to about 450 nanometers.

7. The mask of claim 6 wherein said lighting conditions comprise a wavelength of about 193 nanometers and said depression is about 48 nanometers deep.

8. The mask of claim 5 wherein said transparent material comprises quartz.

9. A method of making a semiconductor manufacturing mask, comprising the steps of:

providing a transparent base material;

providing said base material with an attenuating layer;

patterning said attenuating layer with a resist layer, said resist layer patterned to expose a portion of said base material; and

etching, at said exposed portion, a depression to a depth effective in generating a 0-π-phase conflict mark under ambient lighting conditions of use, said mark positioned to align with a corresponding mark on a semiconductor wafer.

10. The method of claim 9 wherein said ambient lighting conditions comprise an illumination wavelength of from about 150 to about 450 nanometers.

11. The method of claim 10 wherein said wavelength is about 193 nanometers.

12. The method of claim 11 wherein said depression is about 48 nanometers in depth.

13. The method of claim 9 wherein said transparent material is quartz.